ABSTRACT

The present invention discloses a chip-stacked package is disclosed. The chip-stacked package comprises: a doubly down-set leadframe having a down-set tip to be wire-bonded; a first semiconductor chip attached under the down-set tip of the leadframe; a first metal wire electrically connecting bonding pads of the first semiconductor chip with the down-set tip of the leadframe; a second semiconductor chip attached on the leadframe; a second metal wire electrically connecting the second semiconductor chip with the leadframe; and an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing the backside of the first semiconductor chip. According to the present invention, since the chip-stacked package is manufactured using the general LOC leadframe, a manufacturing process thereof can be simplified as compared to the existing chip-stacked package. Moreover, the manufacturing process of the chip-stacked package can be simplified while the manufacturing costs of the package can be reduced by virtue of the use of the inexpensive leadframe.